CMH5X16G1E60Z36A2

DDR5 UDIMM OEM

Key Features

- DDR5, Vengeance RGB, 6000MHz, CAS 36, 16GB, single rank.
- 288-pin, dual in-line memory module. (DIMM).
- Utilizes high performance DRAM ICs thoroughly tested for maximum interoperability and reliability.
- Base SPD setting of 4800MHz 40-40-40-77 (t_{CL}-t_{RCD}-t_{RP}-t_{RAS}), 1.1V and EXPO & XMP settings of 6000MHz 36-44-44-96 (t_{CL}-t_{RCD}-t_{RP}-t_{RAS}), 1.4V.
- PMIC Type: Standard PMIC.
- 100% tested at 6000MHz in a 1 DIMM per channel configuration.
- Designed for use in qualified DDR5 laptop.
- Guaranteed operation 2-up. Two years warranty.
- RoHS Compliant.

Revision History

Revision	Date	Description
1.0	Jan 2023	Initial Release

Ordering Information

Part Number	CMH5X16G1E60Z36A2
UPC	840006679899
Description	16GB, DDR5, UDIMM, single rank, RoHS compliant
Shipping Dimension	331 x 215 x 46mm
Shipping Weight	1.23 Kg (25x modules in 1 FG box)
Master Pack Quantity	16x FG Box in 1 Master Shipper, total 400 modules
Master Pack Dimension	690 x 366 x 295mm
Master Pack Weight	21 Kg

Notes:

1. Ordering the standard production part number allows Corsair to fulfill the order with any DRAM that has passed Corsair's rigorous internal qualification requirements for this product. If you have additional version control requirements, please contact your Corsair Sales Representative.

General Description

The CMH5X16G1B60Z36A2 is an 16GB DDR5 SDRAM DIMM modules. The CMH5X16G1B60C36A2-CN is bulk packaged in a 25-unit.

The CMH5X16G1B60Z36A2 is verified to operate in up to 1 DIMM per channel configuration (i.e., 4-up in four channel platforms, 2-up in two channel platforms) at 6000MHz with latencies of 36-44-44-96 (t_{CAS} – t_{RCD} – t_{RP} – t_{RAS}) at 1.4V through the SPD (Serial Presence Detect) settings contained on the module.

Best of Corsair's engineering

Corsair performs rigorous testing and screening on all components to select only the best for Corsair modules. The tests check for high frequency and/or low latency capabilities for each IC. Then, they are thoroughly tested for maximum interoperability and reliability as a united group to meet the stringent design criteria demanded by performance computing and gaming users.

DDR5 UDIMM Connector Pin Assignments

Pin#	Front Side	Pin#	Back Side
1	VIN_BULK	145	VIN_BULK
2	RFU	146	VIN_BULK
3	RFU	147	PWR_GOOD
4	HSCL	148	HSA
5	HSDA	149	RFU
6	VSS	150	VSS
7	RFU	151	PWR_EN
8	VSS	152	RFU
9	DQ0_A	153	VSS
10	VSS	154	DQ2_A
11	DQ1_A	155	VSS
12	VSS	156	DQ3_A
13	DQS0_A_c	157	VSS
14	DQS0_A_t	158	DM0_A_n
15	VSS	159	VSS
16	DQ4_A	160	DQ6_A
17	VSS	161	VSS
18	DQ5_A	162	DQ7_A
19	VSS	163	VSS
20	DQ8_A	164	DQ10_A
21	VSS	165	VSS
22	DQ9_A	166	DQ11_A
23	VSS	167	VSS
24	DM1_A_n	168	DQS1_A_c
25	VSS	169	DQS1_A_t
26	DQ12_A	170	VSS
27	VSS	171	DQ14_A
28	DQ13_A	172	VSS
29	VSS	173	DQ15_A
30	DQ16_A	174	VSS
31	VSS	175	DQ18_A
32	DQ17_A	176	VSS
33	VSS	177	DQ19_A
34	DQS2_A_c	178	VSS
35	DQS2_A_t	179	DM2_A_n
36	VSS	180	VSS

Pin#	Front Side	Pin#	Back Side
75	RFU	219	RFU
KEY			
76	RFU	220	RFU
77	VSS	221	VSS
78	CK0_B_t	222	CK1_B_t
79	CK0_B_c	223	CK1_B_c
80	VSS	224	VSS
81	RFU	225	RFU
82	CA12_B	226	RFU
83	VSS	227	VSS
84	CA10_B	228	CA11_B
85	CA8_B	229	CA9_B
86	VSS	230	VSS
87	CA6_B	231	CA7_B
88	CA4_B	232	CA5_B
89	VSS	233	VSS
90	CA2_B	234	CA3_B
91	CA0_B	235	CA1_B
92	VSS	236	VSS
93	CS0_B_n	237	CS1_B_n
94	VSS	238	VSS
95	RESET_n	239	DQS4_B_c
96	VSS	240	DQS4_B_t
97	CB0_B	241	VSS
98	VSS	242	CB2_B
99	CB1_B	243	VSS
100	VSS	244	CB3_B
101	DQ0_B	245	VSS
102	VSS	246	DQ2_B
103	DQ1_B	247	VSS
104	VSS	248	DQ3_B
105	DQS0_B_c	249	VSS
106	DQS0_B_t	250	DM0_B_n
107	VSS	251	VSS
108	DQ4_B	252	DQ6_B
109	VSS	253	VSS

37	DQ20_A	181	DQ22_A
38	VSS	182	VSS
39	DQ21_A	183	DQ23_A
40	VSS	184	VSS
41	DQ24_A	185	DQ26_A
42	VSS	186	VSS
43	DQ25_A	187	DQ27_A
44	VSS	188	VSS
45	DM3_A_n	189	DQS3_A_c
46	VSS	190	DQS3_A_t
47	DQ28_A	191	VSS
48	VSS	192	DQ30_A
49	DQ29_A	193	VSS
50	VSS	194	DQ31_A
51	CB0_A	195	VSS
52	VSS	196	CB2_A
53	CB1_A	197	VSS
54	VSS	198	CB3_A
55	DQS4_A_c	199	VSS
56	DQS4_A_t	200	ALERT_n
57	VSS	201	VSS
58	CS0_A_n	202	CS1_A_n
59	VSS	203	VSS
60	CA0_A	204	CA1_A
61	CA2_A	205	CA3_A
62	VSS	206	VSS
63	CA4_A	207	CA5_A
64	CA6_A	208	CA7_A
65	VSS	209	VSS
66	CA8_A	210	CA9_A
67	CA10_A	211	CA11_A
68	VSS	212	VSS
69	CA12_A	213	RFU
70	RFU	214	RFU
71	VSS	215	VSS
72	CK0_A_t	216	CK1_A_t
73	CK0_A_c	217	CK1_A_c
74	VSS	218	VSS

110	DQ5_B	254	DQ7_B
111	VSS	255	VSS
112	DQ8_B	256	DQ10_B
113	VSS	257	VSS
114	DQ9_B	258	DQ11_B
115	VSS	259	VSS
116	DM1_B_n	260	DQS1_B_c
117	VSS	261	DQS1_B_t
118	DQ12_B	262	VSS
119	VSS	263	DQ14_B
120	DQ13_B	264	VSS
121	VSS	265	DQ15_B
122	DQ16_B	266	VSS
123	VSS	267	DQ18_B
124	DQ17_B	268	VSS
125	VSS	269	DQ19_B
126	DQS2_B_c	270	VSS
127	DQS2_B_t	271	DM2_B_n
128	VSS	272	VSS
129	DQ20_B	273	DQ22_B
130	VSS	274	VSS
131	DQ21_B	275	DQ23_B
132	VSS	276	VSS
133	DQ24_B	277	DQ26_B
134	VSS	278	VSS
135	DQ25_B	279	DQ27_B
136	VSS	280	VSS
137	DM3_B_n	281	DQS3_B_c
138	VSS	282	DQS3_B_t
139	DQ28_B	283	VSS
140	VSS	284	DQ30_B
141	DQ29_B	285	VSS
142	VSS	286	DQ31_B
143	RFU	287	VSS
144	RFU	288	RFU

Connector Pinout and Signal Description

Pin Definition

Pin Name	Description	Pin Name	Description
CA0_A – CA12_A, CA0_B – CA12_B	SDRAM Command/Address bus	HSCL	SidebandBus clock
CS0_A_n – CS1_A_n, CS0_B_n – CS1_B_n	SDRAM Chip Select	HSDA	SidebandBus data
DQ0_A – DQ31_A, DQ0_B – DQ31_B	DIMM memory data bus	HSA	SidebandBus address
CB0_A – CB3_A, CB0_B – CB3_B	DIMM ECC check bits	ALERT_n	SDRAM ALERT_n
DQS0_A_t – DQS4_A_t, DQS0_B_t – DQS4_B_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set DRAMs to a Known State
DQS0_A_c – DQS4_A_c, DQS0_B_c – DQS4_B_c	SDRAM data strobes (negative line of differential pair)	VIN_BULK	5 V power input supply to the PMIC for analog circuits
DM0_A_n – DM3_A_n, DM0_B_n – DM3_B_n	SDRAM data masks	VSS	Power supply return (ground)
CK0_A_t, CK1_A_t, CK0_B_t, CK1_B_t	SDRAM clocks (positive line of differential pair)	PWR_GOOD	Power good indicator
CK0_A_c, CK1_A_c, CK0_B_c, CK1_B_c	SDRAM clocks (negative line of differential pair)	PWR_EN	PMIC Enable
		RFU	Reserved for future use

Note:
DDR5 UDIMM has 2 channels (channel-A and channel-B) of signal bus.
The signals with suffix: _A (e.g. DQ0_A) are for channel-A, and the signals with suffix: _B (e.g. DQ0_B) are for channel-B

Input/Output Functional Description

Symbol	Type	I/O Level	Function
CK0_A_t, CK0_A_c CK1_A_t, CK1_A_c, CK0_B_t, CK0_B_c CK1_B_t, CK1_B_c	Input	VDD	Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c.
CA0_A - CA12_A, CA0_B –CA12_B	Input	VDD	Command/Address Inputs: CA signals provide the command and address inputs according to the Command Truth Table. Note: Since some commands are multi cycle, the pins may not be interchanged between devices on the same bus.
CS0_A_n – CS1_A_n CS0_B_n – CS1_B_n	Input	VDD	Chip Select: All commands are masked when CS_n is registered HIGH. CS_n provides for external Rank selection on systems with multiple Ranks. CS_n is considered part of the command code. CS_n is also used to enter and exit the parts from power down modes.
DQ0_A – DQ31_A DQ0_B – DQ31_B	Input/ Output	VDDQ	Data Input/Output: Bi-directional data bus. If CRC is enabled via Mode Register, then CRC code is added at the end of Data Burst.
CB0_A – CB3_A CB0_B – CB3_B	Input/ Output	VDDQ	DIMM ECC check bits
DQS0_A_t – DQS4_A_t DQS0_A_c – DQS4_A_c DQS0_B_t – DQS4_B_t DQS0_B_c – DQS4_B_c	Input/ Output	VDDQ	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. DDR5 SDRAM supports differential data strobe only and does not support single-ended.
DM0_A_n – DM3_A_n DM0_B_n – DM3_B_n	Input	VDDQ	Input Data Mask: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a Write access. DM_n is sampled on both edges of DQS. For x8 device, the function of DM_n is enabled by MR5:OP[5]=1.
ALERT_n	Input/ Output	VDD	Alert: If there is error in CRC, then Alert_n goes LOW for the period time interval and goes back HIGH. During Connectivity Test mode, this pin works as input. Using this signal or not is dependent on system. In case of not connected as Signal, ALERT_n Pin must be bounded to VDDQ on board.
RESET_n	Input	VDDQ	Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. RESET_n is a CMOS rail to rail signal with DC high and low at 80% and 20% of VDDQ,

Symbol	Type	I/O Level	Function
HSCL	Input	1.0V	Host SidebandBus bus clock, supplied by the controller.
HSDA	Input/ Output	1.0V	Host SidebandBus data, connected from the controller to Hubs or Host bus Target devices.
HSA	Input	2.1V (max)	Host SidebandBus bus device ID address pin; input to a Hub or other client device to distinguish between identical devices in the I3C-Basic address range.
RFU			Reserved for Future Use. No on DIMM electrical connection is present.
PWR_GOOD	Input/ Output	Open Drain	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceed the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
PWR_EN	Input	3.3V	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This signal is connected to PMIC's VR_EN pin.
VIN_BULK	Supply	5V	5 V power input supply to the PMIC for analog circuits.
VSS	Supply		Ground

SPD Data

Listed below is data contained in the SPD EEPROM of the CMH5X16G1B60C36A2-CN

SPD Byte	Description	Decimal Equiv	Hex Value
0	Number of Bytes in SPD Device	48	30
1	SPD Revision	16	10
2	Key Byte / Host Bus Command Protocol Type	18	12
3	Key Byte / Module Type	2	02
4	First SDRAM Density and Package	4	04
5	First SDRAM Addressing	0	00
6	First SDRAM I/O Width	32	20
7	First SDRAM Bank Groups & Banks Per Bank Group	98	62
8	Second SDRAM Density and Package	4	04
9	Second SDRAM Addressing	0	00
10	Second SDRAM I/O Width	32	20
11	Second SDRAM Bank Groups & Banks Per Bank Group	98	62
12	SDRAM Optional Features	96	60
13	Thermal and Refresh Options	0	00
14	Reserved	0	00
15	Reserved	0	00
16	SDRAM Nominal Voltage, VDD	0	00
17	SDRAM Nominal Voltage, VDDQ	0	00
18	SDRAM Nominal Voltage, VPP	0	00
19	Reserved	0	00
20	SDRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte	160	A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte	1	01
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte	242	F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte	3	03
24	CAS Latencies Supported, First Byte	114	72
25	CAS Latencies Supported, Second Byte	13	0D
26	CAS Latencies Supported, Third Byte	0	00
27	CAS Latencies Supported, Fourth Byte	0	00
28	CAS Latencies Supported, Fifth Byte	0	00
29	Reserved	0	00
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	26	1A
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte	65	41
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Least Significant Byte	26	1A
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Most Significant Byte	65	41
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), Least SignificantByte	26	1A
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), Most Significant Byte	65	41
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	0	00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Most Significant Byte	125	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	26	1A
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Most Significant Byte	190	BE
40	SDRAM Minimum Write Recovery Time (tWRmin), Least Significant Byte	48	30
41	SDRAM Minimum Write Recovery Time (tWRmin), Most Significant Byte	117	75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Least Significant Byte	39	27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Most Significant Byte	1	01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Least Significant Byte	160	A0

45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Most Significant Byte	0	00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Least Significant Byte	130	82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsb_dlr min), Most Significant Byte	0	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min), Least Significant Byte	0	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min), Most Significant Byte	0	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min), Least Significant Byte	0	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min), Most Significant Byte	0	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min), Least Significant Byte	0	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min), Most Significant Byte	0	00
54	SDRAM Refresh Management, First Byte, First SDRAM	0	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	0	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	0	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	0	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	0	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	0	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	0	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	0	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	0	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	0	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	0	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	0	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	0	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	0	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	0	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	0	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group(tRRD_Lmin), Least Significant Byte	136	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group(tRRD_Lmin), Most Significant Byte	19	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group(tRRD_Lmin), Lower Clock Limit	8	08
73	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group(tCCD_Lmin), Least Significant Byte	136	88
74	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group(tCCD_Lmin), Most Significant Byte	19	13
75	SDRAM Minimum Read to Read Command Delay Time, Same Bank Group(tCCD_Lmin), Lower Clock Limit	8	08
76	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group(tCCD_L_WRmin), Least Significant Byte	32	20
77	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group(tCCD_L_WRmin), Most Significant Byte	78	4E
78	SDRAM Minimum Write to Write Command Delay Time, Same Bank Group(tCCD_L_WRmin), Lower Clock Limit	32	20
79	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group(tCCD_L_WR2min), Least Significant Byte	16	10
80	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group(tCCD_L_WR2min), Most Significant Byte	39	27

81	SDRAM Minimum Write to Write Command Delay Time, Second Write not RMW, Same Bank Group(tCCD_L_WR2min), Lower Clock Limit	16	10
82	SDRAM Minimum Four Activate Window (tFAWmin), Least Significant Byte	21	15
83	SDRAM Minimum Four Activate Window (tFAWmin), Most Significant Byte	52	34
84	SDRAM Minimum Four Activate Window (tFAWmin), Lower Clock Limit	32	20
85	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group,(tCCD_L_WTRmin), Least Significant Byte	16	10
86	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group,(tCCD_L_WTRmin), Most Significant Byte	39	27
87	SDRAM Minimum Write to Read Command Delay Time, Same Bank Group,(tCCD_L_WTRmin), Lower Clock Limit	16	10
88	SDRAM Minimum Write to Read Command Delay Time, Different BankGroup, (tCCD_S_WTRmin), Least Significant Byte	196	C4
89	SDRAM Minimum Write to Read Command Delay Time, Different BankGroup, (tCCD_S_WTRmin), Most Significant Byte	9	09
90	SDRAM Minimum Write to Read Command Delay Time, Different BankGroup, (tCCD_S_WTRmin), Lower Clock Limit	4	04
91	SDRAM Minimum Read to Precharge Command Delay Time,(tRTPmin), Least Significant Byte	76	4C
92	SDRAM Minimum Read to Precharge Command Delay Time,(tRTPmin), Most Significant Byte	29	1D
93	SDRAM Minimum Read to Precharge Command Delay Time,(tRTPmin), Lower Clock Limit	12	0C
94	Reserved	0	00
95	Reserved	0	00
96	Reserved	0	00
97	Reserved	0	00
98	Reserved	0	00
99	Reserved	0	00
100	Reserved	0	00
101	Reserved	0	00
102	Reserved	0	00
103	Reserved	0	00
104	Reserved	0	00
105	Reserved	0	00
106	Reserved	0	00
107	Reserved	0	00
108	Reserved	0	00
109	Reserved	0	00
110	Reserved	0	00
111	Reserved	0	00
112	Reserved	0	00
113	Reserved	0	00
114	Reserved	0	00
115	Reserved	0	00
116	Reserved	0	00
117	Reserved	0	00
118	Reserved	0	00
119	Reserved	0	00
120	Reserved	0	00
121	Reserved	0	00
122	Reserved	0	00
123	Reserved	0	00
124	Reserved	0	00
125	Reserved	0	00
126	Reserved	0	00
127	Reserved	0	00

128	Reserved	0	00
129	Reserved	0	00
130	Reserved	0	00
131	Reserved	0	00
132	Reserved	0	00
133	Reserved	0	00
134	Reserved	0	00
135	Reserved	0	00
136	Reserved	0	00
137	Reserved	0	00
138	Reserved	0	00
139	Reserved	0	00
140	Reserved	0	00
141	Reserved	0	00
142	Reserved	0	00
143	Reserved	0	00
144	Reserved	0	00
145	Reserved	0	00
146	Reserved	0	00
147	Reserved	0	00
148	Reserved	0	00
149	Reserved	0	00
150	Reserved	0	00
151	Reserved	0	00
152	Reserved	0	00
153	Reserved	0	00
154	Reserved	0	00
155	Reserved	0	00
156	Reserved	0	00
157	Reserved	0	00
158	Reserved	0	00
159	Reserved	0	00
160	Reserved	0	00
161	Reserved	0	00
162	Reserved	0	00
163	Reserved	0	00
164	Reserved	0	00
165	Reserved	0	00
166	Reserved	0	00
167	Reserved	0	00
168	Reserved	0	00
169	Reserved	0	00
170	Reserved	0	00
171	Reserved	0	00
172	Reserved	0	00
173	Reserved	0	00
174	Reserved	0	00
175	Reserved	0	00
176	Reserved	0	00
177	Reserved	0	00
178	Reserved	0	00
179	Reserved	0	00
180	Reserved	0	00
181	Reserved	0	00

182	Reserved	0	00
183	Reserved	0	00
184	Reserved	0	00
185	Reserved	0	00
186	Reserved	0	00
187	Reserved	0	00
188	Reserved	0	00
189	Reserved	0	00
190	Reserved	0	00
191	Reserved	0	00
192	Reserved	16	10
193	Reserved	0	00
194	SPD Manufacturer ID Code, First Byte	0	00
195	SPD Manufacturer ID Code, Second Byte	0	00
196	SPD Device Type	128	80
197	SPD Device Revision Number	32	20
198	PMIC 0 Manufacturer ID Code, First Byte	0	00
199	PMIC 0 Manufacturer ID Code, Second Byte	0	00
200	PMIC 0 Device Type	130	82
201	PMIC 0 Revision Number	16	10
202	PMIC 1 Manufacturer ID Code, First Byte	0	00
203	PMIC 1 Manufacturer ID Code, Second Byte	0	00
204	PMIC 1 Device Type	0	00
205	PMIC 1 Revision Number	0	00
206	PMIC 2 Manufacturer ID Code, First Byte	0	00
207	PMIC 2 Manufacturer ID Code, Second Byte	0	00
208	PMIC 2 Device Type	0	00
209	PMIC 2 Revision Number	0	00
210	Thermal Sensor Manufacturer ID Code, First Byte	0	00
211	Thermal Sensor Manufacturer ID Code, Second Byte	0	00
212	Thermal Sensor Device Type	0	00
213	Thermal Sensor Revision Number	0	00
214	Reserved	0	00
215	Reserved	0	00
216	Reserved	0	00
217	Reserved	0	00
218	Reserved	0	00
219	Reserved	0	00
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225	Reserved	0	00
226	Reserved	0	00
227	Reserved	0	00
228	Reserved	0	00
229	Reserved	0	00
230	Module Nominal Height	30	1E
231	Module Maximum Thickness	51	33
232	Reference Raw Card Used	0	00
233	DIMM Attributes	133	85
234	Module Organization	0	00
235	Memory Channel Bus Width	34	22

236	Reserved	0	00
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508	Reserved	0	00
509	Reserved	0	00
510	CRC For Bytes 0~509, Least Significant Byte	175	AF
511	CRC For Bytes 0~509, Most Significant Byte	20	14
512	Module Manufacturer's ID Code, First Byte	2	02
513	Module Manufacturer's ID Code, Second Byte	158	9E
514	Module Manufacturing Location	0	00
515	Module Manufacturing Date	0	00
516	Module Manufacturing Date	0	00
517	Module Serial Number	0	00
518	Module Serial Number	0	00
519	Module Serial Number	0	00
520	Module Serial Number	0	00
521	Module Part Number	67	43
522	Module Part Number	77	4D
523	Module Part Number	72	48
524	Module Part Number	53	35
525	Module Part Number	88	58
526	Module Part Number	49	31
527	Module Part Number	54	36
528	Module Part Number	71	47
529	Module Part Number	49	31
530	Module Part Number	66	42
531	Module Part Number	54	36
532	Module Part Number	48	30
533	Module Part Number	67	43
534	Module Part Number	51	33
535	Module Part Number	54	36
536	Module Part Number	65	41
537	Module Part Number	50	32
538	Module Part Number	0	00
539	Module Part Number	0	00
540	Module Part Number	0	00
541	Module Part Number	0	00
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546	Module Part Number	0	00
547	Module Part Number	0	00
548	Module Part Number	0	00
549	Module Part Number	0	00
550	Module Part Number	0	00
551	Module Revision Code	0	00
552	DRAM Manufacturer's ID Code, First Byte	0	00
553	DRAM Manufacturer's ID Code, Second Byte	0	00
554	DRAM Stepping	0	00
555	Module Manufacturer's Specific Data	0	00
556	Module Manufacturer's Specific Data	0	00

557	Module Manufacturer's Specific Data	0	00
558	Module Manufacturer's Specific Data	0	00
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635	Module Manufacturer's Specific Data	0	00
636	Module Manufacturer's Specific Data	0	00
637	Module Manufacturer's Specific Data	0	00
638	Reserved	0	00
639	Reserved	0	00

640	End User Programmable	12	0C
641	End User Programmable	74	4A
642	End User Programmable	48	30
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648	End User Programmable	0	00
649	End User Programmable	18	12
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654	End User Programmable	80	50
655	End User Programmable	114	72
656	End User Programmable	111	6F
657	End User Programmable	102	66
658	End User Programmable	105	69
659	End User Programmable	108	6C
660	End User Programmable	101	65
661	End User Programmable	32	20
662	End User Programmable	49	31
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705	End User Programmable	39	27
706	End User Programmable	39	27
707	End User Programmable	0	00
708	End User Programmable	36	24
709	End User Programmable	77	4D
710	End User Programmable	1	01
711	End User Programmable	122	7A
712	End User Programmable	237	ED
713	End User Programmable	2	02
714	End User Programmable	0	00
715	End User Programmable	0	00
716	End User Programmable	0	00
717	End User Programmable	212	D4
718	End User Programmable	46	2E
719	End User Programmable	212	D4
720	End User Programmable	46	2E
721	End User Programmable	212	D4
722	End User Programmable	46	2E
723	End User Programmable	220	DC
724	End User Programmable	98	62
725	End User Programmable	176	B0
726	End User Programmable	145	91
727	End User Programmable	48	30
728	End User Programmable	117	75
729	End User Programmable	39	27
730	End User Programmable	1	01
731	End User Programmable	160	A0
732	End User Programmable	0	00
733	End User Programmable	130	82
734	End User Programmable	0	00
735	End User Programmable	136	88
736	End User Programmable	19	13
737	End User Programmable	8	08
738	End User Programmable	32	20
739	End User Programmable	78	4E
740	End User Programmable	32	20
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747	End User Programmable	196	C4

748	End User Programmable	9	09
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750	End User Programmable	136	88
751	End User Programmable	19	13
752	End User Programmable	8	08
753	End User Programmable	76	4C
754	End User Programmable	29	1D
755	End User Programmable	12	0C
756	End User Programmable	170	AA
757	End User Programmable	41	29
758	End User Programmable	32	20
759	End User Programmable	0	00
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762	End User Programmable	0	00
763	End User Programmable	3	03
764	End User Programmable	16	10
765	End User Programmable	0	00
766	End User Programmable	194	C2
767	End User Programmable	169	A9
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